

# USB4 2.0 ENGINEERING CHANGE NOTICE FORM

**Title: TMU asymmetric correction wording simplification**  
**Applied to: USB4 Specification Version 2.0**

<b>Brief description of the functional changes:</b>
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This ECN aligns terminology throughout the Gen 4 asymmetric correction section and makes it more coherent and readable. The functionality itself does not change, just the wording.
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<b>Benefits as a result of the changes:</b>
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<u>It simplifies the section description and reduces the likelihood of misunderstanding errors.</u>
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<b>An assessment of the impact to the existing revision and systems that currently conform to the USB specification:</b>
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NA
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<b>An analysis of the hardware implications:</b>
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NA
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<b>An analysis of the software implications:</b>
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NA
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<b>An analysis of the compliance testing implications:</b>
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NA
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## Actual Change

### (a). Section 7.2.3 Asymmetry Corrections

#### To Text:

Time stamps shall be corrected for asymmetry between transmit and receive Paths. An Upstream Facing Port shall correct for asymmetry by performing the following computations:

$$t1 = \text{Delay Request Sent Time Stamp} + \text{TxTimeToWire}$$

$$t4 = \text{Delay Response Received Time Stamp} - \text{RxTimeToWire}$$

$$tu1 = \text{Delay Request Received Time Stamp} - \text{RxTimeStamp} - (\text{Symbols Delay}) \times (\text{Symbol Time}) - \text{RxTimeToWire}$$

$$tu2 = \text{Delay Response Sent Time Stamp} + \text{TxTimeToWire}$$

where, TxTimeToWire is the value in the *TxTimeToWire* field of the TMU\_ADP\_CS\_1 register of the Upstream Facing Port, RxTimeToWire is the value in the *RxTimeToWire* field of the TMU\_ADP\_CS\_2 register of the Upstream Facing Port, and RxTimeStamp is defined below for each Link speed.

*Note: The reference plane is a virtual representation of the RX and TX pipeline depth. The reference plane is constant regardless of whether or not RS-FEC is activated.*

A Downstream Facing Port shall correct for asymmetry by performing the following computations:

$$t2 = \text{Delay Request Received Time Stamp} - \text{RxTimeToWire}$$

$$t3 = \text{Delay Response Sent Time Stamp} + \text{TxTimeToWire}$$

$$td1 = \text{Delay Request Sent Time Stamp} + \text{TxTimeToWire}$$

$$td2 = \text{Delay Response Received Time Stamp} - \text{RxTimeStamp} - (\text{Symbols Delay}) \times (\text{Symbol Time}) - \text{RxTimeToWire}$$

where, TxTimeToWire is the value in the *TxTimeToWire* field of the TMU\_ADP\_CS\_1 register of the Downstream Facing Port, RxTimeToWire is the value in the *RxTimeToWire* field of the TMU\_ADP\_CS\_2 register of the Downstream Facing Port, and RxTimeStamp is defined below for each Link speed.

For a Gen 2 or Gen 3 Link:

- The time duration between when a USB4 Port generates a time stamp and when it transmits first bit of a TSNOS on the wire shall be equal to the value in the *TxTimeToWire* field of the TMU\_ADP\_CS\_1 register.
- The time duration between when a USB4 Port receives the first bit of a TSNOS on the wire and when it generates a time stamp shall be equal to the value in the *RxTimeToWire* field of the TMU\_ADP\_CS\_2 register.
- RxTimeStamp Point is define in Section 7.2.1.
- *Symbols Delay* is 0.

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For a Gen 4 Link:

- The time duration between when a USB4 Port generates a Time Stamp Point and when it transmits first bit of a TSNOS on the wire shall be calculated using Equation 7-1.

## Equation 7-1. Time Difference from Time Stamp Point to TSNOS Transmission

$$\Delta T = (\text{Symbols Delay}) \times (\text{Symbol Time}) + \text{TxTimeToWire}$$

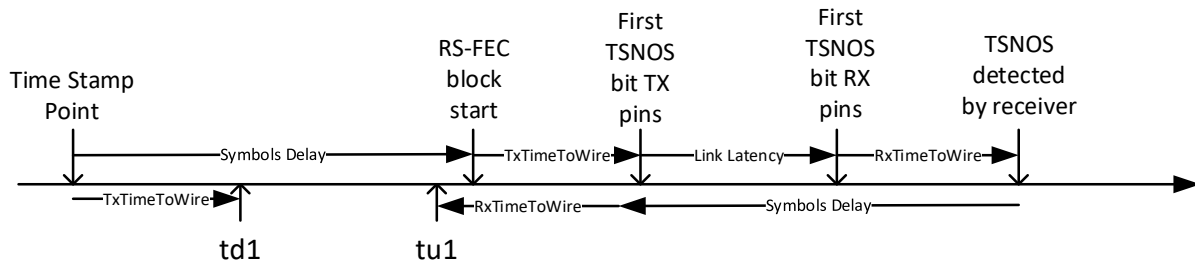
- ~~RxTimeStamp is the time when a USB4 Port detects the first TSNOS, subtracted by the value of the Symbols Delay field multiplied by the Symbol Time.~~
- The time duration between when a USB4 Port receives the first bit of a TSNOS on the wire and when it generates a Time Stamp Point shall be calculated using Equation 7-2.

## Equation 7-2. Time Difference from TSNOS Reception to Time Stamp Point

$$\Delta T = (\text{Symbols Delay}) \times (\text{Symbol Time}) + \text{RxTimeToWire}$$

Figure 7-7 shows an example of how a Downstream Facing Port and an Upstream Facing Port use the TSNOS to generate time stamps for a Gen 4 Link.

**Figure 7-7. Time Stamp Generation using TSNOS for a Gen 4 Link**



*Note: The values in the TxTimeToWire and RxTimeToWire fields are vendor defined.*



## IMPLEMENTATION NOTE

The values of the TxTimeToWire and RxTimeToWire may differ when the Link is operating at different speeds or is on different configurations (e.g. RS-FEC on/off, number of Lanes enabled, and Symmetric/Asymmetric Link).